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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/603,184	06/26/2000	Hirohisa Suzuki	81784.0211	3365

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EXAMINER	
RAMOS FELICIANO, ELISEO	

ART UNIT	PAPER NUMBER
2617	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/603,184	SUZUKI ET AL.	
	Examiner	Art Unit	
	Eliseo Ramos-Feliciano	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2006 (RCE); 09 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Art Unit – Notice

1. The Art Unit location of your application in the USPTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Art Unit 2617.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 9, 2006 (in duplicate January 11, 2006) has been entered.

Claim Rejections - 35 USC § 112

3. Previous rejection to the claims under 35 U.S.C. 112, second paragraph, is withdrawn in view of Applicant's amendment and arguments (from page 6 to first full paragraph in page 7) filed January 9, 2006.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1, 3-9, 11, and 13** are rejected under 35 U.S.C. 102(e) as being anticipated by Tsuji et al. (US Patent Number 6,690,805).

Regarding **claim 1**, Tsuji et al. discloses a noise cancel circuit (Figure 64) for removing noise components in an input audio signal, comprising:

an interpolation circuit (14) for performing interpolation processing on said input audio signal ("AUDIO SIGNAL" from 19),

an LPF (13) for eliminating high frequency components of the input audio signal, an output of the LPF being provided to the interpolation circuit and the interpolation circuit performing an interpolation process on the output from the LPF (column 20, lines 35-57; column 10, lines 48-55), and

a noise detection circuit (20) for detecting the noise portion of said input audio signal, wherein

the input audio signal has a frequency within the audio frequency band (it is in fact an "AUDIO SIGNAL"), and

the noise portion of said input audio signal is replaced by (exchanged – column 21, lines 57-61) an output signal from said interpolation circuit according to an output signal from said noise detection circuit; and

said LPF passes a main signal and eliminates sub-signals and pilot signals (only the low frequency component is extracted; sub-signals and pilot signals are eliminated - column 20, lines 35-57; column 10, lines 48-55).

See Figures 57, 64, 65, 70; column 20, line 35 to column 22, line 57.

Regarding **claim 3**, Tsuji et al. discloses everything claimed as applied above (see *claim 1*). In addition, Tsuji et al. further discloses the noise portion of said input audio signal is interpolated (exchanged) by said interpolation circuit according to an output signal from said noise detection circuit (column 21, lines 57-61). See Figures 57, 64, 65, 70; column 20, line 35 to column 22, line 57.

Regarding **claim 4**, Tsuji et al. discloses everything claimed as applied above (see *claim 3*). In addition, Tsuji et al. further discloses

a first delay circuit (either 15 alone or 15 in combination with 12) for delaying said input audio signal;

a selection circuit (24) for selecting either the output signal from said interpolation circuit or the delayed input audio signal from said first delay circuit, wherein

said selection circuit is controlled according to the output signal from said noise detection circuit (column 21, lines 57-61). See Figures 57, 64, 65, 70; column 20, line 35 to column 22, line 57.

Regarding **claim 5**, Tsuji et al. discloses everything claimed as applied above (see *claim 4*). In addition, Tsuji et al. further discloses wherein said interpolation circuit performs interpolation processing and outputs an interpolation signal regardless of presence or absence of noise components. See Figures 57, 64, 65, 70; column 20, line 35 to column 22, line 57.

Regarding **claim 6**, Tsuji et al. discloses everything claimed as applied above (see *claim 5*). In addition, Tsuji et al. further discloses a second delay circuit (12) for delaying said interpolation signal from said interpolation circuit. See Figures 57, 64, 65, 70; column 20, line 35 to column 22, line 57.

Regarding **claim 7**, Tsuji et al. discloses everything claimed as applied above (see *claim 6*). In addition, Tsuji et al. further discloses wherein said second delay circuit (12) is disposed in a processing stage prior to said interpolation circuit (14) (see Figures 64 or 57).

Regarding **claim 8**, Tsuji et al. discloses everything claimed as applied above (see *claim 6*). In addition, Tsuji et al. further discloses wherein a delay time of said first delay circuit is determined based on a sum of an interpolation processing time of said interpolation circuit and a delay time of said second delay circuit. (The signal is delayed by the delay circuit 15 by an amount to coincide in timing with an output of the interpolation circuit 14 – column 21, lines 49-51. Therefore, because the first delay circuit is the combination of delay 12 and delay 15, the delay time of the first delay circuit is the sum of the interpolation processing time and the delay time of the second delay circuit.)

Regarding **claim 9**, Tsuji et al. discloses everything claimed as applied above (see *claim 8*). In addition, Tsuji et al. further discloses wherein the delay time of said second delay circuit corresponds to a difference obtained by subtracting the interpolation processing time of said interpolation circuit from a time delay between generation and detection of said pulse noise. (Generation and detection of the pulse noise occurs at 20 between "AUDIO SIGNAL" and 24 – see e.g. Figure 64. This includes the delay time of the second delay circuit 12 and the interpolation processing time of the interpolation circuit. Therefore, the difference obtained by subtracting the interpolation processing time of the interpolation circuit from the time delay between generation and detection of the pulse noise corresponds to the delay time of the second delay circuit.)

Regarding **claim 11**, Tsuji et al. discloses everything claimed as applied above (see *claim 1*). In addition, Tsuji et al. further discloses wherein said input audio signal is an FM radio signal (Figure 57, input is FM radio signal; for example, in a car radio – column 1, line 10) (column 20, lines 35-57; column 10, lines 48-55).

Regarding **claim 13**, Tsuji et al. discloses everything claimed as applied above (see *claim 1*). In addition, Tsuji et al. further discloses a switch (24) for changing (exchanged) the noise portion of said input audio signal to the output signal from said interpolation circuit according to the output signal from said noise detection circuit (column 21, lines 57-61). See Figures 57, 64, 65, 70; column 20, line 35 to column 22, line 57.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claim 2 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al. (US Patent Number 6,690,805).

Regarding **claim 2**, Tsuji et al. discloses everything claimed as applied above (see *claim 1*). In addition, Tsuji et al. discloses wherein said interpolation circuit executes polynomial interpolation. However, fails to specify spline interpolation as claimed.

Spline interpolation by definition uses low-degree polynomials in each of the interpolation intervals. Consequently, spline interpolation is a form of polynomial interpolation. Spline interpolation is preferred over polynomial interpolation because the interpolation error

can be made small even when using low degree polynomials for the spline. Thus spline interpolation avoids the problem of Runge's phenomenon which occurs when using high degree polynomials. The spline interpolant is easier to evaluate than the high-degree polynomials used in polynomial interpolation. In terms of computer calculation time, spline interpolation is faster; therefore, less expensive.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use spline interpolation instead of polynomial interpolation because: the interpolation error can be made small even when using low degree polynomials for the spline, avoids the problem of Runge's phenomenon which occurs when using high degree polynomials, is easier to evaluate than the high-degree polynomials used in polynomial interpolation, and is faster in terms of computer calculation time, therefore, less expensive.

Regarding **claim 12**, Tsuji et al. discloses everything claimed as applied above (see *claim 1*). However, fails to specify the claimed timer as part of the same embodiment explained above.

In alternative embodiment, Tsuji et al. discloses a timer (32a – Figure 21 or 35a – Figure 25) for controlling a timing of changing the noise portion of said input audio signal to the output signal from said interpolation circuit (column 16, lines 39-57 and column 17, lines 22-45). Tsuji et al. teaches that the embodiments overlap, therefore, are interchangeable (column 20, lines52-57; column 23, lines 9-14).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide Tsuji et al.'s embodiment explained above with timer for controlling a timing of changing the noise portion of said input audio signal to the output signal

from said interpolation circuit because it is the same Tsuji et al. who teaches that the different embodiments overlap, therefore, are interchangeable.

Response to Arguments

8. Applicant's arguments filed January 9, 2006 have been fully considered but they are not persuasive.

9. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a particular bandpass range, such as the LPF 13 having a bandpass range much lower than that of the argued LPF of the present invention; see Applicant's arguments on page 8, top paragraph) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant's arguments are more specific than claims because the claims do not require a particular bandpass range as argued.

10. Applicant argues that the present invention does not require HPF 21 and high frequency band interpolation circuit 23 employed in Tsuji (see Applicant's arguments on page 8, first full paragraph to end).

In response, it has been noted that claimed language neither excludes argued HPF 21 and high frequency band interpolation circuit 23 because present claim language employs the transitional phrase "comprising", in contrast to "consisting of" as apparently argued. Thus, discussion of HPF 21 and high frequency band interpolation circuit 23 is immaterial to patentability of present claims. See MPEP 2111.03.

Conclusion

11. Any inquiry concerning this communication from the examiner should be directed to Eliseo Ramos-Feliciano whose telephone number is 571-272-7925. The examiner can normally be reached from 8:00 a.m. to 5:30 p.m. on 5-4/9 1st Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha Banks-Harold, can be reached on (571) 272-7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

4/23/06

ELISEO RAMOS-FELICIANO
PRIMARY EXAMINER

ERF/erf
April 23, 2006